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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,177	09/30/2003	Hiroaki Hazama	243444US2	1259

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OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
NGUYEN, VAN THU T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 10/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/673,177	HAZAMA ET AL.
	Examiner	Art Unit
	VanThu Nguyen	2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) *4-7,9* is/are withdrawn from consideration.

5)☒ Claim(s) *8* is/are allowed.

6)☒ Claim(s) *1* is/are rejected.

7)☒ Claim(s) *2 and 3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09/30/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/23/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I, claims 1-3 and 8, in the reply filed on September 2, 2005 is acknowledged. The traversal is on the ground(s) that the combined search will not be a serious burden on Examiner because it is believed with the help of electronic searching, a search may be made of large number of subclasses without substantial effort. This is not found persuasive.

Claims 1 and 8 of Group I recite for limitations of a nonvolatile memory device having structure of a dummy memory cell connected adjacent to select gate transistor of a NAND string.

Claim 4 of Group II recites for particular bias voltages applied to selected gate transistor and adjacent memory cell of a NAND string during data erase.

Claim 9 of Group II recites for particular bias voltages different from that of claim 4 applied to more than one selected gate transistors of plurality of NAND strings.

It is true that with the help of electronic searching, a search may be made with less effort for large number of subclasses. However, the search for Groups I is different from that of Group II and III, and it will be serious burden on Examiner if combined.

The requirement is still deemed proper and is therefore made FINAL.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: NONVOLATILE SEMICONDUCTOR MEMORY DEVICE HAVING CONFIGURATION OF NAND STRINGS WITH DUMMY MEMORY CELLS ADJACENT TO SELECT TRANSISTORS.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Maruyama et al. (U.S. Patent No. 6,188,608, hereafter Maruyama).

Regarding claim 1, Maruyama discloses, in FIG. 5, a nonvolatile semiconductor memory device comprising:

a plurality of electrically rewritable nonvolatile memory cells connected in series (Ma00-DMa01); and

a select gate transistor (TSA20) connected in series to the series-connected memory cells, wherein a memory cell adjacent to said select gate transistor is a dummy cell being out of use for data storage (DMa01).

Allowable Subject Matter

5. Claims 2-3 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claim 8 is allowed.

7. The following is a statement of reasons for the indication of allowance:

The prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Maruyama and Nobukata (5,524,094), taken individually or in combination, do not teach the claimed invention having the following limitations, in combination with the remaining claimed limitations:

(i) wherein said dummy cell is applied with a bias voltage being the same as a bias voltage for remaining memory cells during data erase (as in claim 2); or

(ii) wherein said dummy cell is applied with a bias voltage being the same as a bias voltage of non-selected memory cells in data read and write events (as in claim 3); or

(ii) each said NAND cell unit including memory cells which are located adjacent to the first and second select gate transistors and which are dummy cells being out of use for data storage, wherein said dummy cells are applied with the same bias voltage as that of remaining memory cells during data erase and applied with the same bias voltage as that of non-selected memory cells in data read and write events (as in claim 8).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nobukata et al. (5,524,094) disclose, in FIG. 3, a NAND string gate having two select gate transistors SG0b and SG1b and two end of the string, and a dummy cell connected adjacent to select gate transistor SG1b.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (571) 272-1881. The examiner can normally be reached on Monday-Friday, 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

October 2, 2005

VanThu Nguyen
Primary Examiner
Art Unit 2824